ABSTRACT OF THE DISCLOSURE

[00112] Method and apparatus are provided for facilitating analysis of the intended behavior of a hardware design. According to one embodiment of the present invention, a language-based representation of a hardware design is received. Multiple design verification checks are generated for use in connection with model checking by applying a set of one or more predetermined properties to the language-based representation of the hardware design. Then, the hardware design, as implemented according to the language-based representation, is verified against intended behavior, represented by the set of one or more predetermined properties, by determining whether one or more of the design verification checks are violated by the hardware design. Finally, results of the verification may be reported.

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